



## **iSM002FLKA 2 MBYTE (1024K x 16) CMOS FLASH SIMM**

- **High-Performance**
  - 150 ns Maximum Access Time
  - 13.3 MB/s Read Transfer Rate
- **10,000 Rewrite Cycles Minimum/Component**
- **Flash Electrical Chip-Erase**
  - 2 Second Typical Chip-Erase
- **16  $\mu$ s Typical Word Write**
  - Up to 1 Mb/s Write Transfer Rate
- **Inherent Non-volatility**
  - No Batteries or Disk Required for Back-up
  - 0W Data Retention Power
- **CMOS Low Power Consumption**
  - 20.3 mA Typical Active Current
  - 0.4 mA Typical Standby Current
- **Standard 80-Pin Insertable Module**
  - 0.050 Centerline Lead Spacing
  - Upgrade Path through 128M bytes
- **Hardware Presence Detect**
- **Command Register Architecture for Microprocessor/Microcontroller Compatible Write Interface**
- **Noise Immunity Features**
  - $\pm 10\%$   $V_{CC}$  Tolerance
  - Maximum Latch-Up Immunity Through EPI Processing
- **12.0V  $\pm 5\%$   $V_{pp}$**
- **Integrated Program/Erase Stop Timer**
- **ETOX™ II Nonvolatile Flash Technology**
  - High-Volume Manufacturing Experience

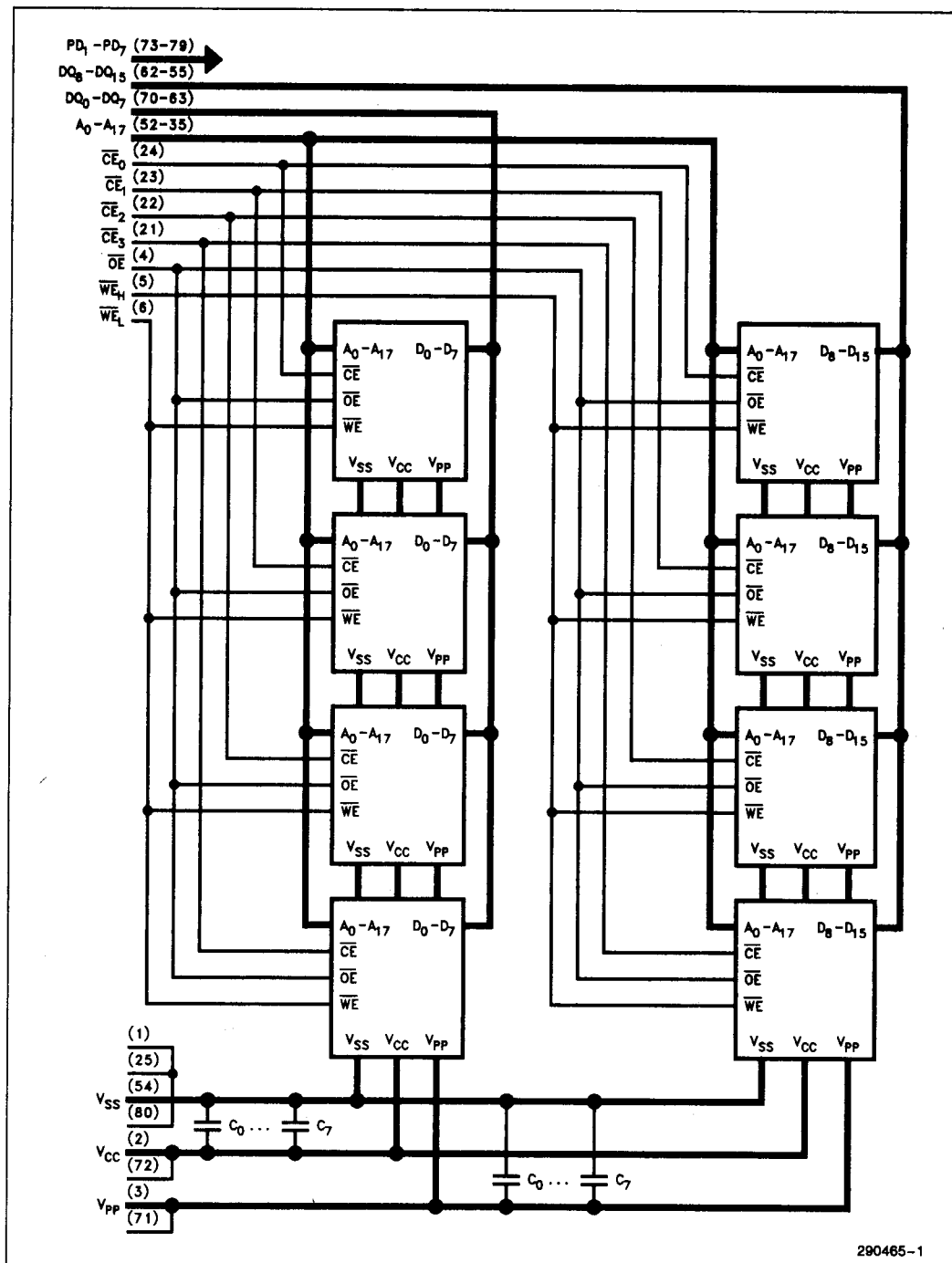
Intel's iSM002FLKA flash SIMM (Single In-Line Memory Module) is targeted at high-density read/write nonvolatile memory. The iSM002FLKA enables you to optimize board space; to offer incremental memory expansion similar to today's DRAM; and to assure continued access to today's and tomorrow's surface-mount technologies. Intel's iSM002FLKA offers a reliable sold-state alternative for mass storage. The flash memory module is also ideal for high performance code and data storage as well as data recording and accumulation.

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The iSM002FLKA, composed of eight 2 Mb flash memories in plastic leaded chip carrier (N28F020), is organized as 1,048,576 words of 16 bits. The PLCCs are mounted, four to a side, together with 0.1  $\mu$ F decoupling capacitors on an 80-pin standard, low-profile module.

Extended erase and program cycling capability is designed into Intel's ETOX™ II (EPROM Tunnel Oxide) process technology. Advanced oxide processing, an optimized tunneling structure, and lower electric field combine to extend reliable cycling beyond that of traditional nonvolatile memory.

Intel's iSM002FLKA flash SIMM employs advanced CMOS circuitry for systems requiring high-performance access speeds, low power consumption, and immunity to noise. Its 150 ns access time provides no WAIT state performance for a wide range of microprocessors and microcontrollers. Maximum standby current of 0.8 mA translates into power savings when the memory module is deselected. Finally, the highest degree of latch-up protection is achieved through Intel's unique EPI processing. Prevention of latch-up is provided for stresses up to 100 mA on address and data pins, from  $-1V$  to  $V_{CC} + 1V$ .



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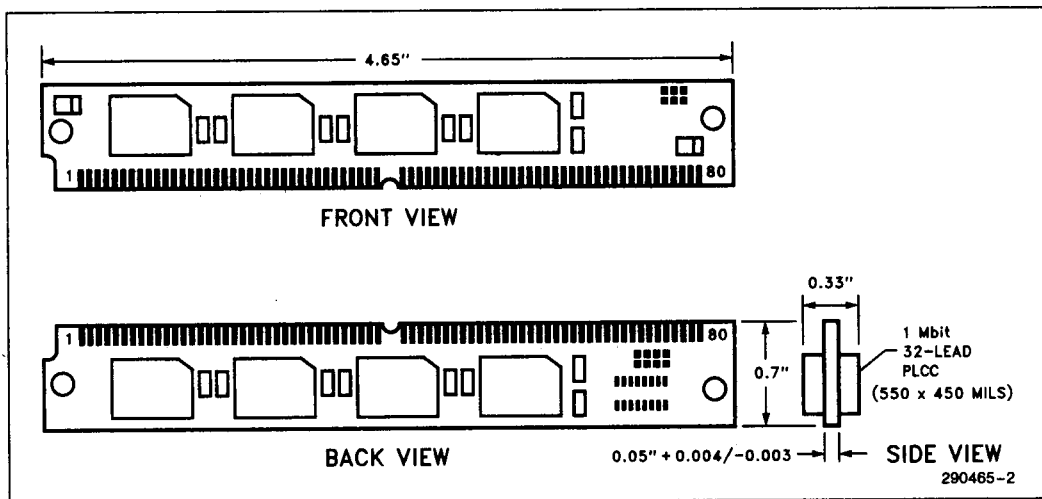


Figure 2. ISM002FLKA Pin Configurations

Table 1. Pinout

1	V <sub>SS</sub>	21	$\overline{OE}3$	41	A <sub>11</sub>	61	DQ <sub>9</sub>
2	V <sub>CC</sub>	22	$\overline{OE}2$	42	A <sub>10</sub>	62	DQ <sub>8</sub>
3	V <sub>PP</sub>	23	$\overline{OE}1$	43	A <sub>9</sub>	63	DQ <sub>7</sub>
4	$\overline{OE}$	24	$\overline{OE}0$	44	A <sub>8</sub>	64	DQ <sub>6</sub>
5	$\overline{WEH}$	25	V <sub>SS</sub>	45	A <sub>7</sub>	65	DQ <sub>5</sub>
6	$\overline{WEL}$	26	RES	46	A <sub>6</sub>	66	DQ <sub>4</sub>
7	NC	27	RES	47	A <sub>5</sub>	67	DQ <sub>3</sub>
8	RES	28	RES	48	A <sub>4</sub>	68	DQ <sub>2</sub>
9	RES	29	RES	49	A <sub>3</sub>	69	DQ <sub>1</sub>
10	RES	30	NC	50	A <sub>2</sub>	70	DQ <sub>0</sub>
11	RES	31	NC	51	A <sub>1</sub>	71	V <sub>PP</sub>
12	RES	32	NC	52	A <sub>0</sub>	72	V <sub>CC</sub>
13	RES	33	NC	53	RES	73	PD <sub>1</sub>
14	RES	34	NC	54	V <sub>SS</sub>	74	PD <sub>2</sub>
15	RES	35	A <sub>17</sub>	55	DQ <sub>15</sub>	75	PD <sub>3</sub>
16	RES	36	A <sub>16</sub>	56	DQ <sub>14</sub>	76	PD <sub>4</sub>
17	NC	37	A <sub>15</sub>	57	DQ <sub>13</sub>	77	PD <sub>5</sub>
18	NC	38	A <sub>14</sub>	58	DQ <sub>12</sub>	78	PD <sub>6</sub>
19	NC	39	A <sub>13</sub>	59	DQ <sub>11</sub>	79	PD <sub>7</sub>
20	NC	40	A <sub>12</sub>	60	DQ <sub>10</sub>	80	V <sub>SS</sub>

Table 2. Pin Description

Symbol	Type	Name and Function																				
A <sub>0</sub> –A <sub>17</sub>	INPUT	<b>ADDRESS INPUTS</b> for memory addresses. Addresses are internally latched during a write cycle.																				
DQ <sub>0</sub> –DQ <sub>15</sub>	INPUT/ OUTPUT	<b>DATA INPUT/OUTPUT:</b> Inputs data during memory write cycles; outputs data during memory read cycles. The data pins are active high and float to tri-state OFF when the chip is deselected or the outputs are disabled. Data is internally latched during a write cycle.																				
$\overline{CE}_0$ – $\overline{CE}_3$	INPUT	<b>CHIP ENABLE:</b> Activates each device's control logic, input buffers, decoders, and sense amplifiers. Each line is unique to one set of 2 devices (word). $\overline{CE}_X$ is active low; $\overline{CE}_X$ high deselects the memory device and reduces power consumption to standby levels. Only one $\overline{CE}_X$ may be active at a time.																				
$\overline{OE}$	INPUT	<b>OUTPUT ENABLE:</b> Gates the devices outputs through the data buffers during a read cycle. $\overline{OE}$ is active low.																				
$\overline{WE}_H$ ; $\overline{WE}_L$	INPUT	<b>WRITE ENABLE</b> controls writes to the control register and the array. ( $\overline{WE}_H$ = High Byte; $\overline{WE}_L$ = Low Byte) Write enable is active low. Addresses are latched on the falling edge and data is latched on the rising edge of the $\overline{WE}$ pulse. <b>NOTE:</b> With $V_{pp} \leq 6.5V$ , memory contents cannot be altered.																				
V <sub>PP</sub>		<b>ERASE/PROGRAM POWER SUPPLY</b> for writing the command register, erasing the entire array, or programming bytes in the array (12V ± 5%).																				
V <sub>CC</sub>		<b>DEVICE POWER SUPPLY:</b> (5V ± 10%).																				
V <sub>SS</sub>		<b>GROUND.</b>																				
NC		<b>NO INTERNAL CONNECTION</b> to device. Pin may be driven or left floating. <table><tr><th>Pin</th><th>Function</th></tr><tr><td>17</td><td><math>\overline{CE}_7</math></td></tr><tr><td>18</td><td><math>\overline{CE}_6</math></td></tr><tr><td>19</td><td><math>\overline{CE}_5</math></td></tr><tr><td>20</td><td><math>\overline{CE}_4</math></td></tr><tr><td>30</td><td>A<sub>22</sub></td></tr><tr><td>31</td><td>A<sub>21</sub></td></tr><tr><td>32</td><td>A<sub>20</sub></td></tr><tr><td>33</td><td>A<sub>19</sub></td></tr><tr><td>34</td><td>A<sub>18</sub></td></tr></table>	Pin	Function	17	$\overline{CE}_7$	18	$\overline{CE}_6$	19	$\overline{CE}_5$	20	$\overline{CE}_4$	30	A <sub>22</sub>	31	A <sub>21</sub>	32	A <sub>20</sub>	33	A <sub>19</sub>	34	A <sub>18</sub>
Pin	Function																					
17	$\overline{CE}_7$																					
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31	A <sub>21</sub>																					
32	A <sub>20</sub>																					
33	A <sub>19</sub>																					
34	A <sub>18</sub>																					
RES		<b>RESERVED</b> for future product enhancements.																				
PD <sub>1</sub> –PD <sub>7</sub>		<b>PRESENCE DETECT:</b> Denotes word depth (512K) and access time of device. See Table 3, "Presence Detect "PD" Pins" on Page 5.																				

Table 3. Presence Detect "PD" Pins

MODULE CAPACITY IDENTIFICATION			
MODULE CAPACITY WORD DEPTH	PD6	PD2	PD1
NO MODULE	O	O	O
256K/32M	O	O	S
512K/64M	O	S	O
1M/128M	O	S	S
2M/256M	S	O	O
4M/512M	S	O	S
8M/1G	S	S	O
16M/2G	S	S	S

MODULE SPEED IDENTIFICATION				
MAXIMUM ACCESS TIME	PD7	PD5	PD4	PD3
> 300 ns	S	S	S	S
300 ns	S	S	S	O
250 ns	S	S	O	S
200 ns	S	S	O	O
185 ns	S	O	S	S
150 ns	S	O	S	O
135 ns	S	O	O	S
120 ns	S	O	O	O
100 ns	O	S	S	S
85 ns	O	S	S	O
70 ns	O	S	O	S
60 ns	O	S	O	O
50 ns	O	O	S	S
40 ns	O	O	S	O
30 ns	O	O	O	S
ND	O	O	O	O

O = OPEN CIRCUIT ON MODULE

S = SHORT CIRCUIT TO GROUND ON MODULE

ND = NOT DEFINED

## SINGLE IN-LINE MEMORY MODULE BOARD

PC substrate: Glass Epoxy [0.05" + 0.004/-0.003 nominal thickness]. The iSM002FLKA low-profile SIMM mounts easily between expansion slots. See Appendix A for a list of 80-pin socket suppliers.

## APPLICATIONS

With high density, nonvolatility, and extended cycling capability, Intel's iSM002FLKA flash SIMMs offer an innovative alternative to disk and battery-backed static RAM.

Primary applications and operating systems can be stored in flash, eliminating the slow disk-to-DRAM download process. Performance is dramatically enhanced and power consumption is reduced—a consideration particularly important in portable equipment. Flexibility is increased with Flash's electrical chip erasure allowing in-system updates to operating systems and application code.

In diskless workstations and terminals, network traffic is reduced to a minimum and systems are instant-on. Reliability exceeds that of electro-mechanical media. Often in these environments, power glitches force extended re-boot periods for all networked terminals. This mishap is no longer an issue if boot code, operating systems, communication protocols and primary applications are flash-resident in each terminal.

For embedded systems that rely on dynamic RAM/disk for main system memory or nonvolatile backup storage, Flash SIMMs provide a solid state alternative in a minimal form factor. Flash memory provides higher performance, lower power consumption and instant-on capability. Additionally, flash is more rugged and reliable in harsh environments where extreme temperatures and shock can cause disk-based systems to fail.

For systems currently using a high-density static RAM/battery configuration for code updates and data accumulation, flash memory's inherent nonvolatility eliminates the need for battery backup. The possibility of battery failure is removed. This consideration is important for portable equipment and medical instruments, both requiring continuous performance. In addition, flash memory offers a four-to-one cost advantage over SRAM.

Flash memory's electrical chip erasure, byte reprogrammability and complete nonvolatility fit well with data accumulation and recording needs. Electrical chip-erasure gives the designer a "blank-slate" in which to log or record data. Data can be periodically off-loaded for analysis-erasing the slate and repeating the cycle.

Flash SIMMs add additional flexibility to designers by offering end-users incremental expansion memory. As code requirements grow or as memory prices drop, your customers have the option of adding more memory.

## PRINCIPALS OF OPERATION

The iSM002FLKA operates as eight N28F020 flash memories connected as shown in the Functional Block Diagram on Page 2.

The iSM002FLKA, organized as 1024K x 16, can also be configured for 8- and 32-bit systems. For 32-bit systems, add a second SIMM to your design as currently done with DRAM. For byte-wide operation, buffer the SIMMs DQ<sub>0</sub>-DQ<sub>7</sub> and DQ<sub>8</sub>-DQ<sub>15</sub> lines with an octal transceiver; then, tie the buffered outputs together to form the 8-bit bus. Decode the transceiver's enable input with an address line.

The iSM002FLKA features hardware presence detect pins to facilitate memory design. The presence detect pins (PD1-PD7) indicate module word depth and maximum access speed (see Table 3 on the previous page). The pins allow memory-specific wait-state generation upon system initialization. To use the presence capability, pull-up the PD1-PD7 lines through a pull-up resistor. Read the lines through a port and select the appropriate memory depth and speed from a PD data table.

In the absence of high voltage on the modules V<sub>pp</sub> pins, the iSM002FLKA is a read-only memory array. Manipulation of the module's control pins yields standard read, standby and output disable functions.

Read, standby and output disable operations are also available when high voltage is applied to the V<sub>pp</sub> pins. In addition, high voltage on the V<sub>pp</sub> pins enables erasure and programming of the module's devices. All functions associated with altering the memory contents of one or more devices—erase, erase verify, program and program verify—are accessed via each flash device's command register.

Commands are written to a device's command register using standard microprocessor write timings. Register contents serve as input to the device's internal state-machine which controls the erase and programming circuitry. Write cycles to a device also internally latch addresses and data needed for programming or erase operations. With the appropriate command written to a device's register, standard microprocessor read timings output array data, access the intelligent identifier codes, or output data for erase and program verification.

Table 4. Bus Operations

Pins		V <sub>PP</sub> (1)	CE	OE	WE	DQ <sub>0</sub> –DQ <sub>15</sub>
Operation						
READ-ONLY	Read	V <sub>PPL</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	Data Out
	Output Disable	V <sub>PPL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	Tri-State
	Standby	V <sub>PPL</sub>	V <sub>IH</sub>	X	X	Tri-State
READ/WRITE	Read	V <sub>PPH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	Data Out <sup>(3)</sup>
	Output Disable	V <sub>PPH</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	Tri-State
	Standby <sup>(4)</sup>	V <sub>PPH</sub>	V <sub>IH</sub>	X	X	Tri-State
	Write	V <sub>PPH</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	Data In <sup>(5)</sup>

**NOTES:**

1. Refer to DC Characteristics. When  $V_{PP} = V_{PPL}$  memory contents can be read but not written or erased.
2. Manufacturer and device codes are accessed via a command register write sequence. Refer to Table 5. All other addresses are low.
3. Read operations with  $V_{PP} = V_{PPH}$  may access array data or the intelligent Identifier™ codes.
4. With  $V_{PP}$  at high voltage, the standby current equals  $I_{CC} + I_{PP}$  (standby).
5. Refer to Table 5 for valid Data-In during a write operation.
6. X can be  $V_{IL}$  or  $V_{IH}$ .

## Integrated Stop Timer

Successive command write cycles define the duration of program and erase operations; specifically, the program or erase time durations are normally terminated by associated program or erase verify commands. An integrated stop timer provides simplified timing control over these operations; thus eliminating the need for maximum program/erase timing specifications. Programming and erase pulse durations are minimums only. When the stop timer terminates a program or erase operation, the device enters an inactive state and remains inactive until receiving the appropriate verify or reset command.

## Write Protection

A device's command register is only active when  $V_{PP}$  is at high voltage. Depending upon the application, the system designer may choose to make the  $V_{PP}$  power supply switchable—available only when memory updates are desired. When  $V_{PP} = V_{PPL}$ , the contents of the register default to the read command, making the iSM002FLKA a read-only memory. In this mode, the memory contents cannot be altered.

Or, the system designer may choose to "hardwire"  $V_{PP}$ , making the high voltage supply constantly available. In this instance, all operations are performed in conjunction with the command register. The iSM002FLKA is designed to accommodate either design practice, and to encourage optimization of flash's processor-memory interface.

The following section first discusses byte-wide organization, building a basic understanding of byte-wide

bus operations, command definitions, and programming and erasure algorithms. The section concludes with performance enhancements for both 16- and 32-bit systems.

## BUS OPERATIONS

### Read

Each of the iSM002FLKA's flash memory devices has two control functions, both of which must be logically active, to obtain data. Chip-Enable ( $\overline{CE}_X$ ) is the power control and should be used for device selection. Four chip enables ( $\overline{CE}_0-\overline{CE}_3$ ) control the array's eight devices. Each line is unique to one set of two devices (word). Only one  $\overline{CE}_X$  may be active at a time.

Output-Enable ( $\overline{OE}$ ) is the output control and should be used to gate data from a device to the output pins on the module, independent of device selection. One  $\overline{OE}$  line serves the iSM002FLKA's flash devices. Figure 7 illustrates read timing waveforms.

When the  $V_{PP}$  lines are high ( $V_{PPH}$ ), a read operation can be used to access array data, to output a device's intelligent identifier™ code, and to access a device's data for program/erase verification. When  $V_{PP}$  is low ( $V_{PPL}$ ), a read operation can **only** access array data.

### Output Disable

With the iSM002FLKA's Output-Enable pin at a logic-high level ( $V_{IH}$ ), outputs from all devices are disabled. They are placed in a high-impedance state.

## STANDBY

With Chip-Enable at a logic-high level, the standby operation disables most of the deselected devices circuitry and substantially reduces device power consumption. The outputs of the deselected devices are placed in a high-impedance state, independent of the Output-Enable signal. If a word is deselected during erase, programming, or program/erase verification, the device draws active current until the operation is terminated.

## Intelligent Identifier Operation

The intelligent identifier operation outputs the selected devices' manufacturer code (89H) and device code (BDH). The manufacturer code and device code are read via the devices' command register. Following a write of 90H to a device's command register, a read from address location 0000H outputs the manufacturer code (89H). A read from address 0001H outputs the device code (BDH).

## Write

Erase and programming is accomplished via each device's command register, when high voltage is applied to the V<sub>pp</sub> pins. The contents of each device's register serve as input to its internal state-machine. The state machine outputs dictate the function of each device.

A device's command register itself does not occupy an addressable memory location. The register is a latch used to store the command, along with address and data information needed to execute the command.

**Two write enable lines are provided,  $\overline{WE}_H$  and  $\overline{WE}_L$ , allowing selective write control of upper and lower bytes.**

A device's command register is written by selecting the device (Chip-Enable low), then bringing Write-Enable ( $\overline{WE}_H$  or  $\overline{WE}_L$ ) to a logic-low level ( $V_{IL}$ ). If both WE lines are a logic low, both upper and lower bytes are written. Addresses are latched on the falling edge of the Write-Enable signal, while data is latched on the rising edge of the Write-Enable pulse. Standard microprocessor write timing are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

## COMMAND DEFINITIONS

When low voltage is applied to the module's V<sub>pp</sub> pins, the contents of all devices' command registers default to 00H, enabling read-only operations.

Placing high voltage on the module's V<sub>pp</sub> pins allows read/write operation on selected devices. Operations are selected by writing specific data patterns to the device(s) command register. Table 5 defines these register commands.

**Table 5. Command Definitions**

Command	Bus Cycles Req'd	First Bus Cycle			Second Bus Cycle		
		Operation(1)	Address(2)	Data(3)	Operation(1)	Address(2)	Data(3)
Read Memory	1	Write	X	00H			
Read intelligent identifier™ Codes(4)	3	Write	X	90H	Read	(4)	(4)
Set-up Erase/Erase(5)	2	Write	X	20H	Write	X	20H
Erase Verify(5)	2	Write	EA	A0H	Read	X	EVD
Set-up Program/Program(6)	2	Write	X	40H	Write	PA	PD
Program Verify(6)	2	Write	X	C0H	Read	X	PVD
Reset(7)	2	Write	X	FFH	Write	X	FFH

### NOTES:

- Bus operations are defined in Table 4.
- IA = Identifier address: 00H for manufacturer code, 01H for device code.  
EA = Address of memory location to be read during erase verify.  
PA = Address of memory location to be programmed.  
Addresses are latched on the falling edge of the Write-Enable pulse.
- ID = Data read from location IA during device identification (Mfr = 89H, Device BDH).  
EVD = Data read from location EA during erase verify.  
PD = Data to be programmed at location PA. Data is latched on the rising edge of Write-Enable.  
PVD = Data read from location PA during program verify. PA is latched on the Program command.
- Following the Read Intelligent ID command, two read operations access manufacturer and device codes.
- Figure 4 illustrates the Quick-Erase™ Algorithm.
- Figure 3 illustrates the Quick-Pulse Programming™ Algorithm.
- The second bus cycle must be followed by the desired command register write.



## Read Command

While  $V_{pp}$  is high, for erasure and programming, the selected devices memory contents can be accessed via the read command. The read operation is initiated by writing 00H into the command register of each device. Microprocessor read cycles retrieve array data. The selected devices remain enabled for reads until their command register contents are altered.

The default contents of each device's command register upon  $V_{pp}$  power-up is 00H. This default value ensures that no spurious alteration to the iSM002FLKA's memory contents occurs during the  $V_{pp}$  power transition. Where the  $V_{pp}$  supply is hard-wired to the iSM002FLKA's  $V_{pp}$  pins, all eight devices power-up and remain enabled for reads until their command-register contents are changed. Refer to the AC Read Characteristics and Waveforms for specific timing parameters.

## Intelligent Identifier Command

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacturer- and device-codes must be accessible while the device resides in the target system.

Each flash memory device contains an intelligent Identifier operation. The operation is initiated by writing 90H into the command register. Following the command write, a read cycle from address 0000H retrieves the manufacturer code of 89H. A read cycle from address 0001H returns the device code of BDH. To terminate the operation, it is necessary to write another valid command into the register.

The intelligent Identifier and the Presence Detect pins give you complementary information. While the PD pins denote speed and depth, the intelligent Identifier operation gives you manufacture and device data.

## Set-Up Erase/Erase Commands

Set-up Erase is a command-only operation that stages a selected device for electrical erasure of all bytes in its array. The set-up erase operation is performed by writing 20H to the command register.

To commence chip-erasure, the erase command (20H) must again be written to the register. The erase operation begins with the rising edge of a Write-Enable pulse ( $\overline{WE}_H$  or  $\overline{WE}_L$ ) and terminates

with the rising edge of the next Write-Enable pulse (i.e., Erase-Verify Command).

This two-step sequence of set-up followed by execution ensures that memory contents are not accidentally erased. Also, chip-erasure can only occur when high voltage is applied to the  $V_{pp}$  pins. In the absence of this high voltage, memory contents are protected against erasure. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

## Erase-Verify Command

The erase command erases all bytes of the selected device(s) in parallel. After each erase operation, all bytes must be verified. The erase verify operation is initiated by writing A0H into the command register of the device. The address for the byte to be verified must be supplied as it is latched on the falling edge of a Write-Enable pulse. The register write terminates the erase operation with the rising edge of its Write-Enable pulse.

Each 28F020 applies an internally-generated margin voltage to the addressed byte. Reading FFH from the addressed byte indicates that all bits in the byte are erased.

The erase-verify command must be written to the command register prior to each byte verification to latch its address. The process continues for each byte of the device until a byte does not return FFH data, or the last address is accessed.

In the case where the data read is not FFH, another erase operation is performed. (Refer to Set-up Erase/Erase). Verification then resumes from the address of the last-verified byte. Once all bytes of the device have been verified, the erase step is complete. The device can be programmed. At this point, the verify operation is terminated by writing a valid command (e.g., Program Set-up) to the command register of the device. Figure 4, the Quick-Erase™ algorithm, illustrates how commands and bus operations are combined to perform electrical erasure of each 28F020. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

## Set-Up Program/Program Commands

Set-up program is a command-only operation that stages a device for byte programming. Writing 40H into the command register of the device performs the set-up operation.

Once the program set-up operation is performed, the next Write-Enable pulse causes a transition to an active programming operation. Addresses are internally latched on the falling edge of the Write-Enable pulse. Data is internally latched on the rising edge of the Write-Enable pulse. The rising edge of Write-Enable also begins the programming operation. The programming operation terminates with the next rising edge of Write-Enable, used to write the program-verify command. Refer to AC Programming Characteristics and Waveforms for specific timing parameters.

### Program-Verify Command

Each 28F020 is programmed on a byte-by-byte basis. Byte programming may occur sequentially or at random. Following each programming operation, the byte just programmed must be verified.

The program-verify operation is initiated by writing C0H into the command register of the device. The register write terminates the programming operation with the rising edge of its Write-Enable pulse. The program-verify operation stages the device for verification of the byte last programmed. No new address information is latched.

Each 28F020 applies an internally-generated margin voltage to the byte. A microprocessor read cycle outputs the data. A successful comparison between the programmed byte and true data means that the byte is successfully programmed. Programming then proceeds to the next desired byte location. Figure 3, the Quick-Pulse Programming algorithm (8-bit Systems), illustrates how commands are combined with bus operations to perform byte programming. Refer to AC Programming Characteristics and Waveforms for specific timing parameters.

### Reset Command

A reset command is provided as a means to safely abort the erase- or program-command sequences to a device. Following either set-up command (erase or program) with two consecutive writes of FFH will safely abort the operation. Memory contents will not be altered. A valid command must then be written to place the device in the desired state.

### EXTENDED ERASE/PROGRAM CYCLING

EEPROM cycling failures have always concerned users. The high electrical field required by thin oxide EEPROMs for tunneling can literally tear apart the oxide at defect regions. To combat this, some suppliers have implemented redundancy schemes, reducing cycling failures to insignificant levels. However, redundancy requires that cell size be doubled—an expensive solution.

Intel has designed extended cycling capability into its ETOX II flash memory technology. Resulting improvements in cycling reliability come without increasing memory cell size or complexity. First, an advanced tunnel oxide increases the charge carrying ability ten-fold. Second, the oxide area per cell subjected to the tunneling electric field is one-tenth that of common EEPROMs, minimizing the probability of oxide defects in the region. Finally, the peak electric field during erasure is approximately 2 MV/cm lower than EEPROM. The lower electric field greatly reduces oxide stress and the probability of failure—increasing time to wearout by a factor of 100,000,000.

Each of the iSM002FLKA's eight 28F020s is specified for a minimum of 10,000 program/erase cycles. Each device is programmed and erased using Intel's Quick-Pulse Programming and Quick-Erase algorithms. Intel's algorithmic approach uses a series of operations (pulses), along with byte verification, to completely and reliably erase and program the device.

For further information, see Reliability Report RR-60 (ETOX II Reliability Data Summary).

### QUICK-PULSE PROGRAMMING ALGORITHM

The Quick-Pulse Programming algorithm uses programming operations of 10  $\mu$ s duration. Each operation is followed by a byte verification to determine when the addressed byte has been successfully programmed. The algorithm allows for up to 25 programming operations per byte, although most bytes verify on the first or second operation. The entire sequence of programming and byte verification is performed with  $V_{pp}$  at high voltage. Figure 3 illustrates the Quick-Pulse Programming algorithm for 8-bit systems.

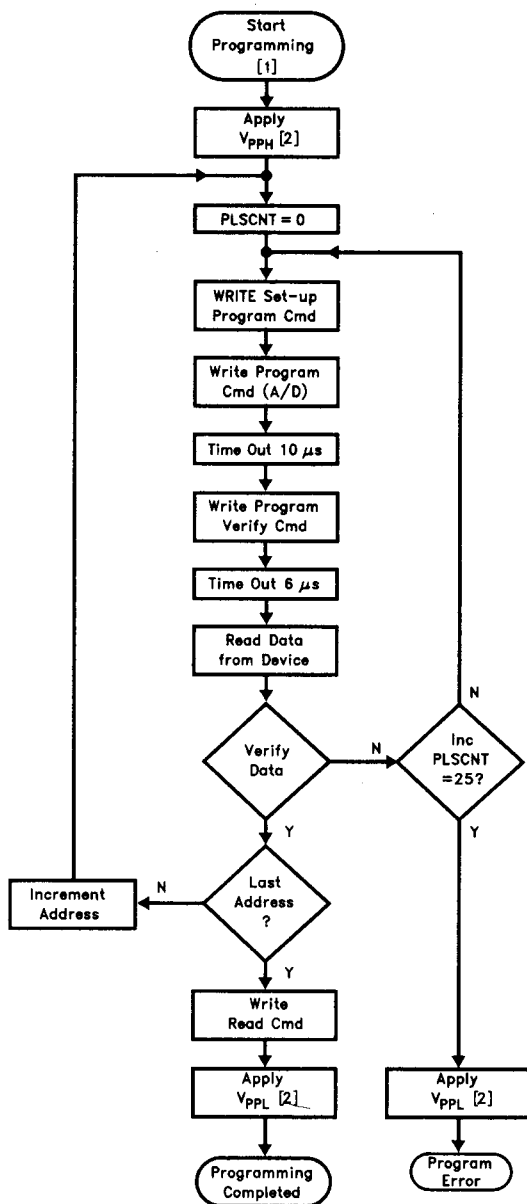
## QUICK-ERASE ALGORITHM

Intel's Quick-Erase algorithm yields fast and reliable electrical erasure of memory contents. The algorithm employs a closed-loop flow, similar to the Quick-Pulse Programming algorithm, to simultaneously remove charge from all bits in the array.

Erasure begins with a read of memory contents. The iSM002FLKA is erased when shipped from the factory. Reading FFH data from each device would immediately be followed by device programming.

For devices being erased and reprogrammed, uniform and reliable erasure is ensured by first programming all bits in the device to their charged state (Data = 00H). This is accomplished, using the Quick-Pulse Programming algorithm, in approximately two seconds.

Erase execution then continues with an initial erase operation. Erase verification (data = FFH) begins at address 0000H and continues through the array to the last address, or until data other than FFH is encountered. With each erase operation, an increasing number of bytes verify to the erased state. Erase efficiency may be improved by storing the address of the last byte verified in a register. Following the next erase operation, verification starts at that stored address location. Erasure typically occurs in one second. Figure 4 illustrates the Quick-Erase algorithm for 8-bit systems.



Bus Operation	Command	Comments
Standby		Wait for V <sub>pp</sub> Ramp to V <sub>ppH</sub> (1)
		Initialize Pulse-Count
Write	Set-up Program	Data = 40H
Write	Program	Valid Address/Data
Standby		Duration of Program Operation (t <sub>WHWH1</sub> )
Write	Program(3) Verify	Data = C0H; Stops Program Operation(4)
Standby		t <sub>WHGL</sub>
Read		Read Byte to Verify Programming
Standby		Compare Data Output to Data Expected
Write	Read	Data = 00H, Resets the Register for Read Operations
Standby		Wait for V <sub>pp</sub> Ramp to V <sub>ppL</sub> (2)

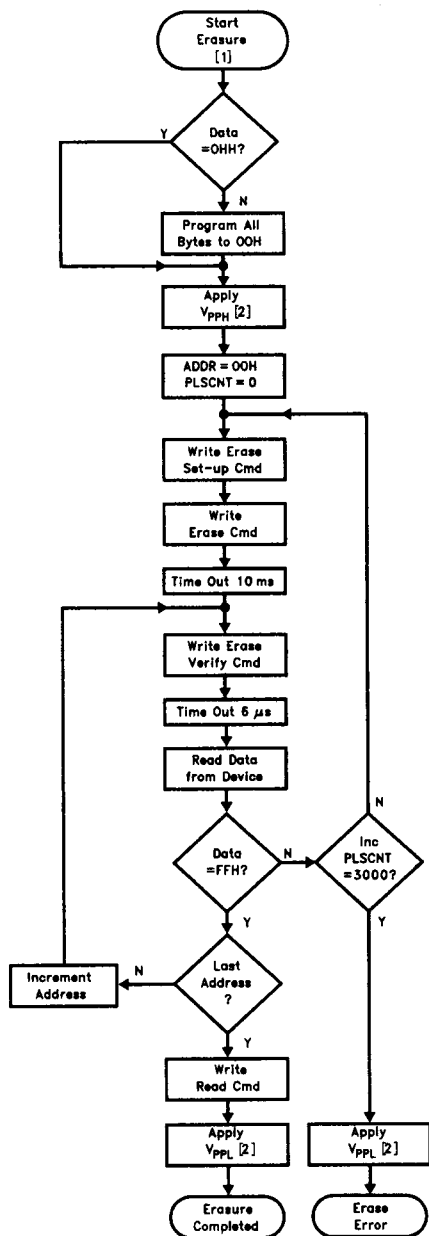
290465-3

**NOTES:**

1. CAUTION: The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.
2. See DC Characteristics for value of V<sub>ppH</sub> and V<sub>ppL</sub>.

3. Program Verify is only performed after byte programming. A final read/compare may be performed (optional) after the register is written with the Read command.
4. Refer to principles of operation

**Figure 3. Quick-Pulse Programming Algorithm (8-Bit Systems)**



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**NOTES:**

1. **CAUTION:** The algorithm **MUST BE FOLLOWED** to ensure proper and reliable operation of the device.
2. See DC Characteristics for value of  $V_{ppH}$  and  $V_{ppL}$ .

Bus Operation	Command	Comments
Standby		Entire Memory Must = 00H Before Erasure
		Use Quick-Pulse Programming™ Algorithm (Figure 4)
		Wait for $V_{pp}$ Ramp to $V_{ppH}(2)$
Write	Set-up Erase	Data = 20H
	Erase	Data = 20H
Standby		Duration of Erase Operation ( $t_{WHWH2}$ )
Write	Erase(3) Verify	Addr = Byte to Verify; Data = A0H; Stops Erase Operation(4)
Standby		$t_{WHGL}$
Read		Read Byte to Verify Erasure
Standby		Compare Output to FFH Increment Pulse-Count
Write	Read	Data = 00H, Resets the Register for Read Operations
Standby		Wait for $V_{pp}$ Ramp to $V_{ppL}(2)$

3. Erase Verify is performed only after chip-erase. A final read/compare may be performed (optional) after the register is written with the read command.
4. Refer to principles of operation.

**Figure 4. Quick-Erase Algorithm (8-Bit Systems)**

## HIGH PERFORMANCE PARALLEL DEVICE ERASURE

Total erase time for the iSM002FLKA is reduced by implementing a parallel erase algorithm (Note 1). You save time by erasing all devices at the same time. However, since flash memories may erase at different rates, you must verify each device separately. This can be done in a word-wise fashion with the command register Reset command and a special masking algorithm.

Take for example the case of two-device (parallel) erasure. The CPU first writes the data word erase command 2020h twice in succession. This starts erasure. After 10 ms, the CPU writes the data word verify command A0A0h to stop erasure and setup erase verification. If both bytes are erased at the given address, then the CPU increments the address (by 2) and then writes the verify command A0A0h again. If neither byte is erased, then the CPU issues the erase sequence again without incrementing the address.

Suppose at the given address only the low byte verifies FFh data? Could the whole chip be erased? The answer is yes. Rather than check the rest of the low byte addresses independently of the high byte, simply use the reset command to mask the low byte from erasure and erase verification on the next erase loop. In this example the erase command would be 20FFh and the verify command would be A0FFh. Once the high byte verifies at that address, the CPU modifies the command back to the default 2020h and A0A0h, increments the address by 2, and writes the verify command to the next address.

See Figure 5 for a conceptual view of the parallel erase flow chart and Appendix B for the detailed version. These flow charts are for 16-bit systems and can be expanded for 32-bit designs.

### NOTE:

1. Parallel Erasure and Programming require appropriate choice of  $V_{PP}$  supply to support the increased power consumption.

## HIGH PERFORMANCE PARALLEL DEVICE PROGRAMMING

Software for word- or double-word programming can be written in two different manners. The first method offers simplicity of design and minimizes software overhead by using a byte programming routine on each device independently (using host CPU's byte addressing mode). The second method offers higher performance by programming the word or double-word data in parallel. This method manipulates the command register instructions for independent byte control. See Figure 6 for conceptual 2-device parallel programming flow chart and Appendix C for the detailed version. Here you can use the host CPU's appropriate word- or double-word addressing modes (i.e., incrementing by 2- or 4-byte addresses, respectively).

### NOTE:

Word or double-word programming assumes 2 or 4 8-bit flash memory devices.

### Parallel Programming Algorithm Summary:

- Decreases programming time by programming 2 flash memories (16 bits) in parallel. The algorithm can be expanded for 32-bit systems.
- Eliminates tracking of high/low byte addresses and respective number of program pulses by directing the CPU to write data-words (16-bit) to the command register.
- Maintains word write and read operations. Should a byte on one device program prior to a byte on the other, the CPU continues to write word-commands to both devices. However, it deselects the verified byte with software commands. An alternative is to independently program high and low bytes using hardware select capability (byte-addressing mode of host CPU).

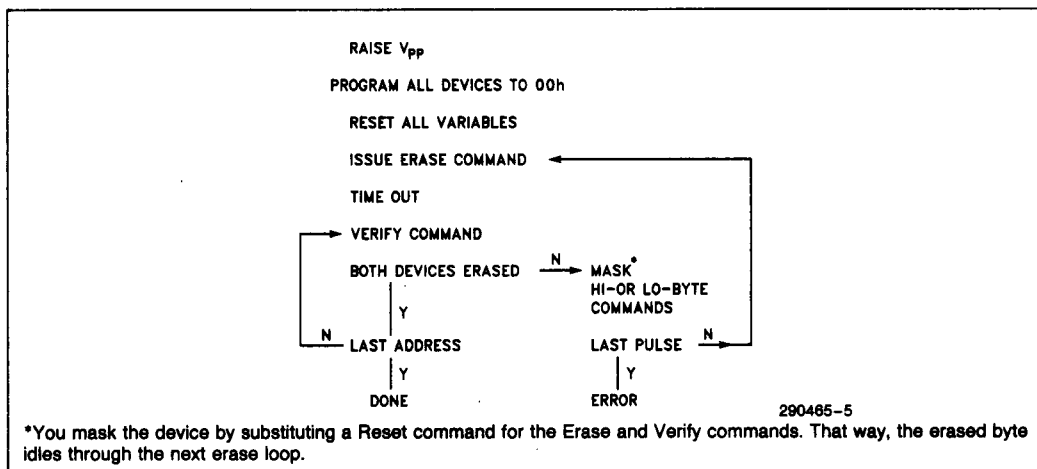


Figure 5. High Performance Parallel Erasure (Conceptual Overview)

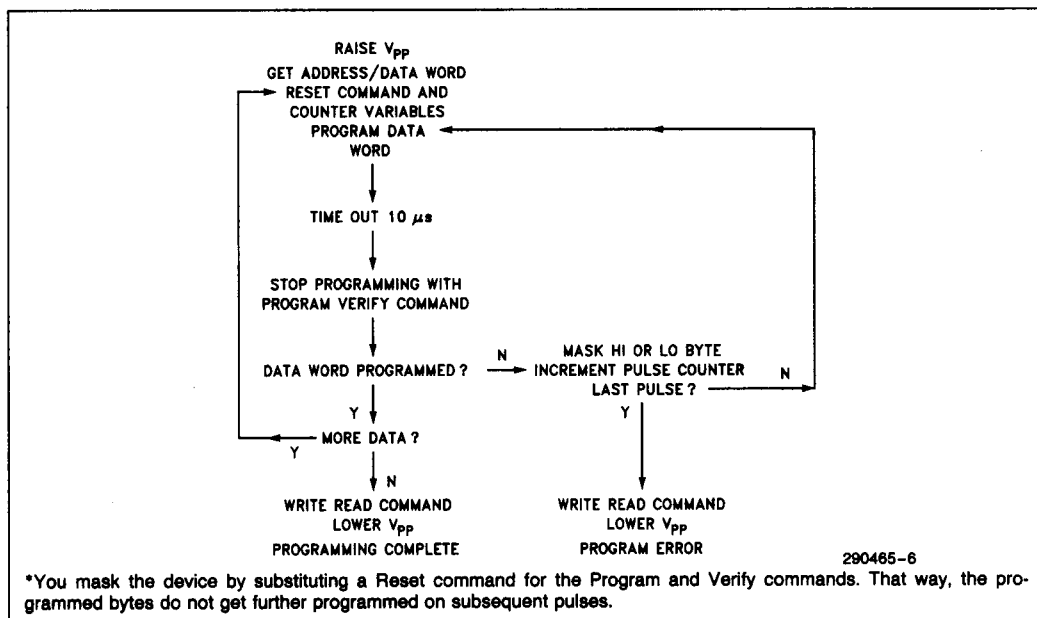


Figure 6. Parallel Programming Flow Chart (Conceptual Overview)

## DESIGN CONSIDERATIONS

### Two-Line Output Control

Two-line control provides for:

- the lowest possible memory power dissipation and,
- complete assurance that output bus contention will not occur.

To efficiently use these two control inputs, an address-decoder output should drive chip-enable, while the system's read signal controls all flash-memories and other parallel memories. This assures that only enabled memory devices have active outputs, while deselected devices maintain the low power standby condition.

### Power Supply Decoupling

Flash-memory power-switching characteristics require careful device decoupling. System designers are interested in three supply current ( $I_{CC}$ ) issues—standby, active, and transient current peaks produced by falling and rising edges of chip-enable. The capacitive and inductive loads on the device outputs determine the magnitudes of these peaks.

Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. The iSM002FLKA features a 0.1  $\mu$ F ceramic capacitor connected between  $V_{CC}$  and  $V_{SS}$ , and between  $V_{PP}$  and  $V_{SS}$ .

Also, a 4.7  $\mu$ F tantalum capacitor decouples the array's power supply between  $V_{CC}$  and  $V_{SS}$  and between  $V_{PP}$  and  $V_{SS}$ . The bulk capacitors will overcome voltage slumps caused by printed-circuit-board trace inductance, and will supply charge to the smaller capacitors as needed.

### V<sub>PP</sub> Trace on Printed Circuit Boards

Programming flash memories, while they reside in the target system, requires that the printed circuit board designer pay attention to the  $V_{PP}$  power supply trace. The two  $V_{PP}$  pins supply current for programming. Use similar trace widths and layout considerations given the  $V_{CC}$  power bus. Adequate  $V_{PP}$  supply traces and decoupling will decrease  $V_{PP}$  voltage spikes and overshoots. Be sure to connect both module  $V_{PP}$  inputs to your 12V supply.

### Power Up/Down Protection

The iSM002FLKA is designed to offer protection against accidental erasure or programming during power transitions. Upon power-up, each 28F020 is indifferent as to which power supply,  $V_{PP}$  or  $V_{CC}$ , powers up first. Power supply sequencing is not required. Internal circuitry in each 28F020 ensures that the command register is reset to the read mode on power up.

A system designer must guard against active writes for  $V_{CC}$  voltages above  $V_{LKO}$  when  $V_{PP}$  is active. Since both  $WE$  and  $CE$  must be low for a command write, driving either to  $V_{IH}$  will inhibit writes. The control register architecture provides an added level of protection since alteration of memory contents only occurs after successful completion of the two-step command sequences.

### Power Dissipation

When designing portable systems, designers must consider battery power consumption not only during device operation, but also for data retention during system idle time. Flash nonvolatility increases the usable battery life of your system because each 28F020 does not consume any power to retain code or data when the system is off. Table 4 illustrates the power dissipated when updating each 28F020.

**Table 4. 28F020 Typical Update Power Dissipation(4)**

Operation	Power Dissipation (Watt-Seconds)
Array Program/Program Verify(1)	0.34
Array Erase/Erase Verify(2)	0.37
One Complete Cycle(3)	1.05

#### NOTES:

- Formula to calculate typical Program/Program Verify Power =  $[V_{PP} \times \# \text{ Bytes} \times \text{typical } \# \text{ Prog Pulses} (t_{WHWH1} \times I_{PP2} \text{ typical} + t_{WHGL} \times I_{PP4} \text{ typical})] + [V_{CC} \times \# \text{ Bytes} \times \text{typical } \# \text{ Prog Pulses} (t_{WHWH1} \times I_{CC2} \text{ typical} + t_{WHGL} \times I_{CC4} \text{ typical})]$ .
- Formula to calculate typical Erase/Erase Verify Power =  $[V_{PP} (V_{PP3} \text{ typical} \times t_{ERASE} \text{ typical} + I_{PP5} \text{ typical} \times t_{WHGL} \times \# \text{ Bytes})] + [V_{CC} (I_{CC3} \text{ typical} \times t_{ERASE} \text{ typical} + I_{CC5} \text{ typical} \times t_{WHGL} \times \# \text{ Bytes})]$ .
- One Complete Cycle = Array Preprogram + Array Erase + Program.
- "Typicals are not guaranteed but based on a limited number of samples taken from production lots.



## ABSOLUTE MAXIMUM RATINGS\*

Operating Temperature  
 During Read ..... 0°C to +70°C<sup>(1)</sup>  
 During Erase/Program ..... 0°C to +70°C  
 Temperature Under Bias ..... -10°C to +80°C  
 Storage Temperature ..... -50°C to +100°C  
 Voltage on Any Pin with  
 Respect to Ground ..... -2.0V to +7.0V<sup>(2)</sup>  
 $V_{PP}$  Supply Voltage with  
 Respect to Ground  
 During Erase/Program .... -2.0V to +14.0V<sup>(2, 3)</sup>  
 $V_{CC}$  Supply Voltage with  
 Respect to Ground ..... -2.0V to +7.0V<sup>(2)</sup>  
 Output Short Circuit Current ..... 100 mA<sup>(4)</sup>

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

*\*WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

### NOTES:

1. Operating temperature is for commercial product defined by this specification.
2. Minimum DC input voltage is -0.5V. During transitions, inputs may undershoot to -2.0V for periods less than 20 ns. Maximum DC voltage on output pins is  $V_{CC} + 0.5V$ , which may overshoot to  $V_{CC} + 2.0V$  for periods less than 20 ns.
3. Maximum DC voltage on  $V_{PP}$  may overshoot to +14.0V for periods less than 20 ns.
4. Output shorted for no more than one second. No more than one output shorted at a time.

## OPERATING CONDITIONS

Symbol	Parameter	Limits		Unit	Comments
		Min	Max		
$T_A$	Operating Temperature	0	70	°C	For Read-Only and Read/Write Operations
$V_{CC}$	$V_{CC}$ Supply Voltage	4.50	5.50	V	

# DC CHARACTERISTICS—TTL/NMOS COMPATIBLE

Symbol	Parameter	Notes	Limits			Unit	Test Conditions
			Min	Typ	Max		
$I_{LI}$	Input Leakage Current	3			$\pm 8.0$	$\mu A$	$V_{CC} = V_{CC} \text{ Max}$ $V_{IN} = V_{CC} \text{ or } V_{SS}$
$I_{LO}$	Output Leakage Current	3			$\pm 40.0$	$\mu A$	$V_{CC} = V_{CC} \text{ Max}$ $V_{OUT} = V_{CC} \text{ or } V_{SS}$
$I_{CCS}$	$V_{CC}$ Standby Current	1, 3			8.0	mA	$V_{CC} = V_{CC} \text{ Max}$ $CE = V_{IH}$
$I_{CC1}$	$V_{CC}$ Active Read Current	2, 3		26	66	mA	$V_{CC} = V_{CC} \text{ Max}$ , $CE = V_{IL}$ $f = 6 \text{ MHz}$ , $I_{OUT} = 0 \text{ mA}$
$I_{CC2}$	$V_{CC}$ Programming Current	2, 3		8.0	26	mA	Programming in Progress
$I_{CC3}$	$V_{CC}$ Erase Current	2, 3		16.0	36	mA	Erase in Progress
$I_{CC4}$	$V_{CC}$ Program Verify Current	2, 3		16.0	36	mA	$V_{PP} = V_{PPH}$ Program Verify in Progress
$I_{CC5}$	$V_{CC}$ Erase Verify Current	2, 3		16.0	36	mA	$V_{PP} = V_{PPH}$ Erase Verify in Progress
$I_{PPS}$	$V_{PP}$ Leakage Current	3			$\pm 80$	$\mu A$	$V_{PP} \leq V_{CC}$
$I_{PP1}$	$V_{PP}$ Read Current or Standby Current	3		0.7	1.6	mA	$V_{PP} > V_{CC}$
					$\pm 80$	$\mu A$	$V_{PP} \leq V_{CC}$
$I_{PP2}$	$V_{PP}$ Programming Current	2, 3		16.5	61.2	mA	$V_{PP} = V_{PPH}$ Programming in Progress
$I_{PP3}$	$V_{PP}$ Erase Current	2, 3		20.5	61.2	mA	$V_{PP} = V_{PPH}$ Erase in Progress
$I_{PP4}$	$V_{PP}$ Program Verify Current	2, 3		4.5	11.2	mA	$V_{PP} = V_{PPH}$ Program Verify in Progress
$I_{PP5}$	$V_{PP}$ Erase Verify Current	2, 3		4.5	11.2	mA	$V_{PP} = V_{PPH}$ Erase Verify in Progress
$V_{IL}$	Input Low Voltage		-0.5		0.8	V	
$V_{IH}$	Input High Voltage		2.0		$V_{CC} + 0.5$	V	
$V_{OL}$	Output Low Voltage				0.45	V	$I_{OL} = 5.8 \text{ mA}$ $V_{CC} = V_{CC} \text{ Min}$
$V_{OH1}$	Output High Voltage		2.4			V	$I_{OH} = -2.5 \text{ mA}$ $V_{CC} = V_{CC} \text{ Min}$
$V_{PPL}$	$V_{PP}$ during Read-Only Operations		0.00		6.5	V	<b>NOTE:</b> Erase/Program are inhibited when $V_{PP} = V_{PPL}$
$V_{PPH}$	$V_{PP}$ during Read/Write Operations		11.40		12.60	V	
$V_{LKO}$	$V_{CC}$ Erase/Write Lock Voltage		2.5			V	

## NOTES:

1.  $V_{CC}$  standby current for 8 devices.

2. Calculations assume only the 2 devices of the 16-bit word are enabled. The remaining 6 devices are in standby.

Current will be higher if interleaving is used.

3. All currents are in RMS unless otherwise noted. Typical values at  $V_{CC} = 5.0V$ ,  $V_{PP} = 12.0V$ ,  $T = 25^{\circ}C$ . These currents are valid for all product versions (packages and speeds).

# DC CHARACTERISTICS—CMOS COMPATIBLE

Symbol	Parameter	Notes	Limits			Unit	Test Conditions
			Min	Typ	Max		
$I_{LI}$	Input Leakage Current	3			$\pm 8.0$	$\mu A$	$V_{CC} = V_{CC} \text{ Max}$ $V_{IN} = V_{CC} \text{ or } V_{SS}$
$I_{LO}$	Output Leakage Current	3			$\pm 40.0$	$\mu A$	$V_{CC} = V_{CC} \text{ Max}$ $V_{OUT} = V_{CC} \text{ or } V_{SS}$
$I_{CCS}$	$V_{CC}$ Standby Current	1, 3		0.4	0.8	mA	$V_{CC} = V_{CC} \text{ Max}$ $CE = V_{CC} \pm 0.2V$
$I_{CC1}$	$V_{CC}$ Active Read Current	2, 3		20.3	60.6	mA	$V_{CC} = V_{CC} \text{ Max}$ , $CE = V_{IL}$ $f = 6 \text{ MHz}$ , $I_{OUT} = 0 \text{ mA}$
$I_{CC2}$	$V_{CC}$ Programming Current	2, 3		2.3	20.6	mA	Programming in Progress
$I_{CC3}$	$V_{CC}$ Erase Current	2, 3		10.3	30.6	mA	Erase in Progress
$I_{CC4}$	$V_{CC}$ Program Verify Current	2, 3		10.3	30.6	mA	$V_{PP} = V_{PPH}$ Program Verify in Progress
$I_{CC5}$	$V_{CC}$ Erase Verify Current	2, 3		10.3	30.6	mA	$V_{PP} = V_{PPH}$ Erase Verify in Progress
$I_{PPS}$	$V_{PP}$ Leakage Current				$\pm 80$	$\mu A$	$V_{PP} \leq V_{CC}$
$I_{PP1}$	$V_{PP}$ Read Current or Standby Current	3		0.7	1.6	mA	$V_{PP} > V_{CC}$
					$\pm 80$	$\mu A$	$V_{PP} \leq V_{CC}$
$I_{PP2}$	$V_{PP}$ Programming Current	2, 3		16.5	61.2	mA	$V_{PP} = V_{PPH}$ Programming in Progress
$I_{PP3}$	$V_{PP}$ Erase Current	2, 3		20.5	61.2	mA	$V_{PP} = V_{PPH}$ Erase in Progress
$I_{PP4}$	$V_{PP}$ Program Verify Current	2, 3		4.5	11.2	mA	$V_{PP} = V_{PPH}$ Program Verify in Progress
$I_{PP5}$	$V_{PP}$ Erase Verify Current	2, 3		4.5	11.2	mA	$V_{PP} = V_{PPH}$ Erase Verify in Progress
$V_{IL}$	Input Low Voltage		-0.5		0.8	V	
$V_{IH}$	Input High Voltage		$0.7 V_{CC}$		$V_{CC} + 0.5$	V	
$V_{OL}$	Output Low Voltage				0.45	V	$I_{OL} = 5.8 \text{ mA}$ $V_{CC} = V_{CC} \text{ Min}$
$V_{OH1}$	Output High Voltage		$0.85 V_{CC}$			V	$I_{OH} = -2.5 \text{ mA}$ , $V_{CC} = V_{CC} \text{ Min}$
$V_{OH2}$			$V_{CC} - 0.4$				$I_{OH} = -100 \mu A$ , $V_{CC} = V_{CC} \text{ Min}$
$V_{PPL}$	$V_{PP}$ during Read-Only Operations		0.00		6.5	V	<b>NOTE:</b> Erase/Program are inhibited when $V_{PP} = V_{PPL}$
$V_{PPH}$	$V_{PP}$ during Read/Write Operations		11.40		12.60	V	
$V_{LKO}$	$V_{CC}$ Erase/Write Lock Voltage		2.5			V	

## NOTES:

- $V_{CC}$  standby current for 8 devices.
- Calculations assume only the 2 devices of the 16-bit word are enabled. The remaining 6 devices are in standby. Current will be higher if interleaving is used.
- All currents are in RMS unless otherwise noted. Typical values at  $V_{CC} = 5.0V$ ,  $V_{PP} = 12.0V$ ,  $T = 25^{\circ}C$ . These currents are valid for all product versions (packages and speeds).

**CAPACITANCE(1)**  $T_A = 25^\circ\text{C}$ ,  $f = 1.0\text{ MHz}$

Symbol	Parameter	Notes	Limits		Unit	Conditions
			Min	Max		
$C_{IN1}$	Address Capacitance	2		60	pF	$V_{IN} = 0V$
$C_{IN2}$	Control Capacitance	2		65	pF	$V_{IN} = 0V$
$C_{OUT}$	Output Capacitance	2		55	pF	$V_{OUT} = 0V$

**NOTES:**

1. Trace capacitance calculated, not measured.
2. Address and control capacitance of a typical device is 6 pF.
3. Output capacitance of a typical device is 12 pF.

**AC TEST CONDITIONS**

Input Rise and Fall Times (10% to 90%) ..... 10 ns  
 Input Pulse Levels ..... 0.45V and 2.4V  
 Input Timing Reference Level ..... 0.8V and 2.0V  
 Output Timing Reference Level ..... 0.8V and 2.0V

**AC CHARACTERISTICS—Read-Only Operations(2)**

Versions		Notes	ISM002FLKA-150		Unit
Symbol	Characteristic		Min	Max	
$t_{AVAV}/t_{RC}$	Read Cycle Time	3	150		ns
$t_{ELQV}/t_{CE}$	Chip Enable Access Time			150	ns
$t_{AVQV}/t_{ACC}$	Address Access Time			150	ns
$t_{GLQV}/t_{OE}$	Output Enable Access Time			55	ns
$t_{ELQX}/t_{LZ}$	Chip Enable to Output in Low Z	3	0		ns
$t_{EHQZ}$	Chip Disable to Output in High Z	3		55	ns
$t_{GLQX}/t_{OLZ}$	Output Enable to Output in Low Z	3	0		ns
$t_{GHQZ}/t_{DF}$	Output Disable to Output in High Z	4		35	ns
$t_{OH}$	Output Hold from Address, $\overline{CE}$ , or $\overline{OE}$ Change	3	0		ns
$t_{WHGL}$	Write Recovery Time before Read		6		$\mu\text{s}$

**NOTES:**

1. Whichever occurs first.
2. Rise/Fall Time  $\leq 10\text{ ns}$ .
3. Not 100% tested: Characterization data available.
4. Guaranteed by design.



### Figure 7. AC Waveforms for Read Operations

## AC CHARACTERISTICS—Write/Erase/Program Operations(1, 2)

Versions			ISM002FLKA-150		Unit
Symbol	Characteristic	Notes	Min	Max	
t <sub>AVAV</sub> /t <sub>WC</sub>	Write Cycle Time		150		ns
t <sub>AVWL</sub> /t <sub>AS</sub>	Address Set-up Time		0		ns
t <sub>WLAX</sub> /t <sub>AH</sub>	Address Hold Time		60		ns
t <sub>DVWH</sub> /t <sub>DS</sub>	Data Set-up Time		50		ns
t <sub>WHDH</sub> /t <sub>DH</sub>	Data Hold Time		10		ns
t <sub>WHGL</sub>	Write Recovery Time before Read		6		μs
t <sub>GHWL</sub>	Read Recovery Time before Write		0		μs
t <sub>ELWL</sub> /t <sub>CS</sub>	Chip Enable Set-up Time before Write		20		ns
t <sub>WEH</sub> /t <sub>CH</sub>	Chip Enable Hold Time		0		ns
t <sub>WLWH</sub> /t <sub>WP</sub>	Write Pulse Width	2	60		ns
t <sub>WHWL</sub> /t <sub>WPH</sub>	Write Pulse Width High		20		ns
t <sub>WHWH1</sub>	Duration of Programming Operation	3	10		μs
t <sub>WHWH2</sub>	Duration of Erase Operation	3	9.5		ms
t <sub>VPEL</sub>	V <sub>PP</sub> Set-up Time to Chip Enable Low		1.0		μs

### NOTES:

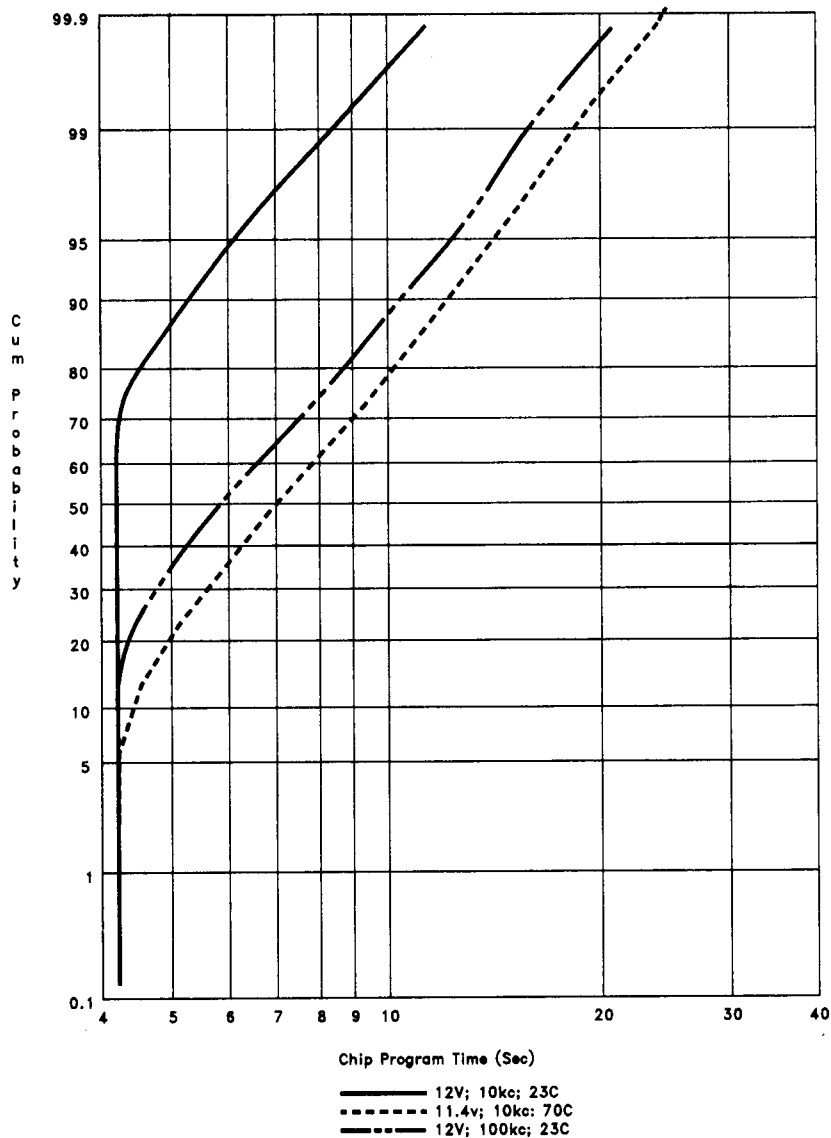
1. Read timing characteristics during read/write operations are the same as during read-only operations. Refer to AC Characteristics for Read-Only Operations.
2. Rise/Fall time ≤ 10 ns.
3. The integrated stop timer terminates the program/erase operations, thereby eliminating the need for a maximum specification.

## ERASE AND PROGRAMMING PERFORMANCE

Parameter	Notes	Limits			Unit
		28F020-150			
		Min	Typ	Max	
Chip Erase Time	1, 3, 4		2	30	Sec
Chip Program Time	1, 2, 4		4	25	Sec
Erase/Program Cycles	1, 5	10,000	100,000		Cycles

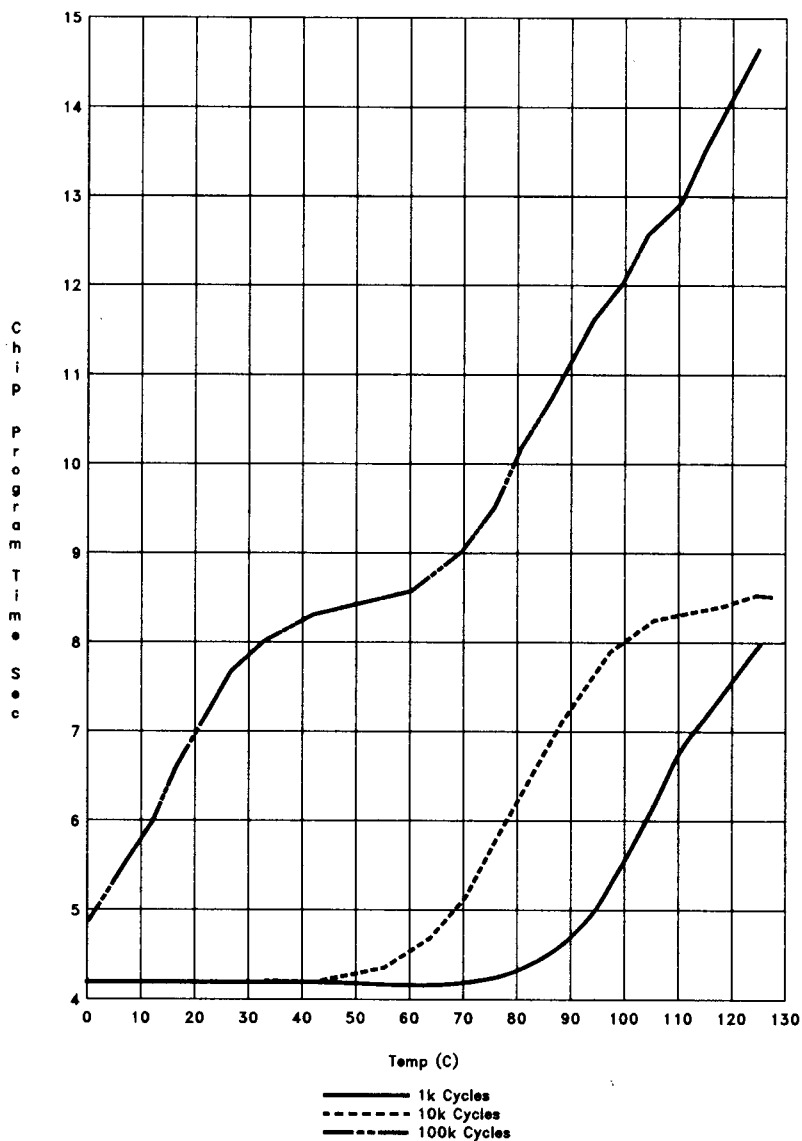
### NOTES:

1. Typicals are not guaranteed, but based on a limited number of samples from production lots. Data taken at 25°C, 12.0V V<sub>PP</sub>.
2. Minimum byte programming time excluding system overhead is 16 μs (10 μs program + 6 μs write recovery), while maximum is 400 μs/byte (16 μs x 25 loops allowed by algorithm). Max chip programming time is specified lower than the worst case allowed by the programming algorithm since most bytes program significantly faster than the worst case byte.
3. Excludes 00H Programming prior to Erasure.
4. Excludes System-Level Overhead.
5. Refer to RR-60 "ETOX™II Flash Memory Reliability Data Summary" for typical cycling data and failure rate calculations.



290465-8

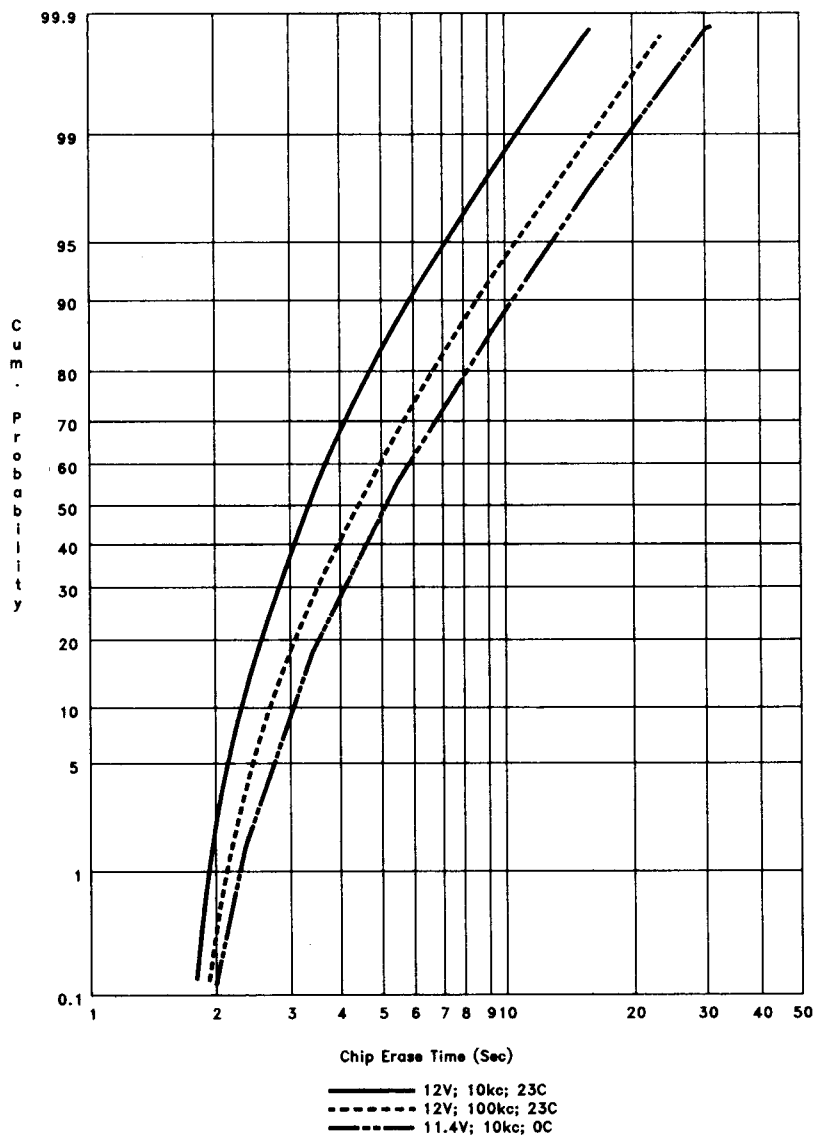
Figure 8. 28F020 Typical Programming Capability



290465-9

Figure 9. 28F020 Typical Program Time at 12V

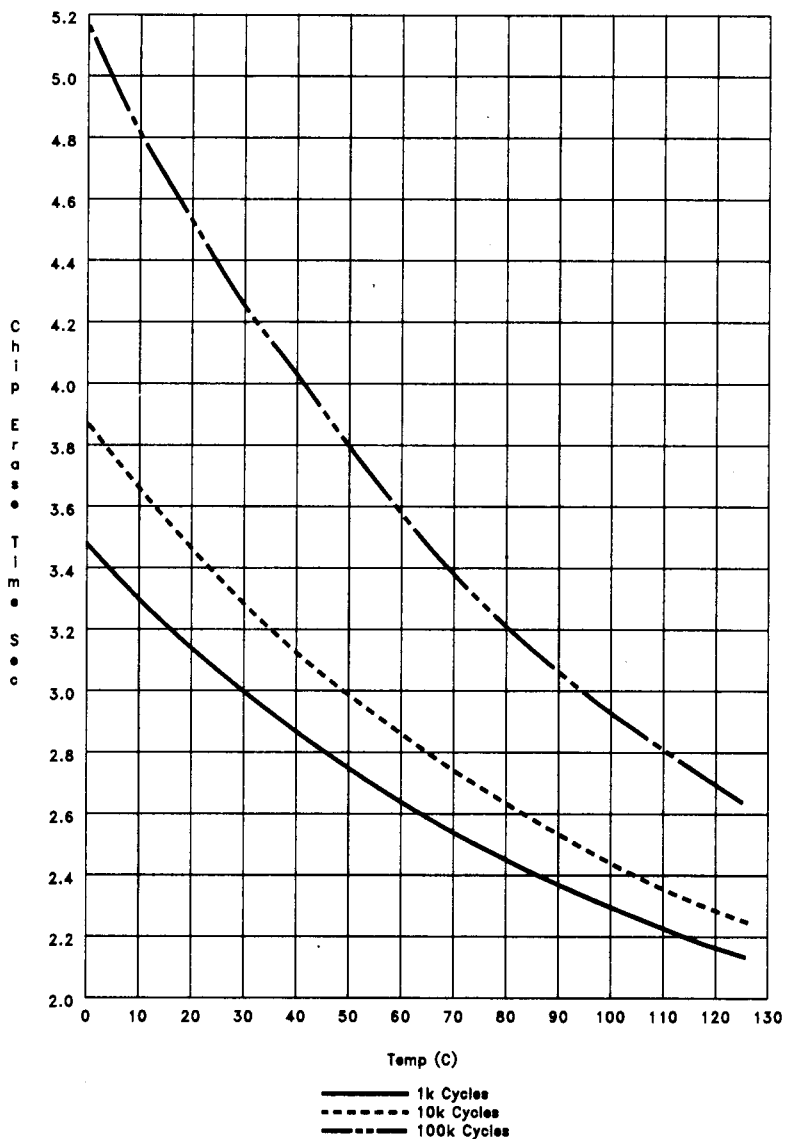




290465-10

**NOTE:**  
Does not include Pre-Erase Program.

**Figure 10. 28F020 Typical Erase Capability**



290465-11

**NOTE:**  
Does not include Pre-Erase Program.

**Figure 11. 28F020 Typical Erase Time at 12.0V**



### Figure 12. AC Waveforms for Programming Operations



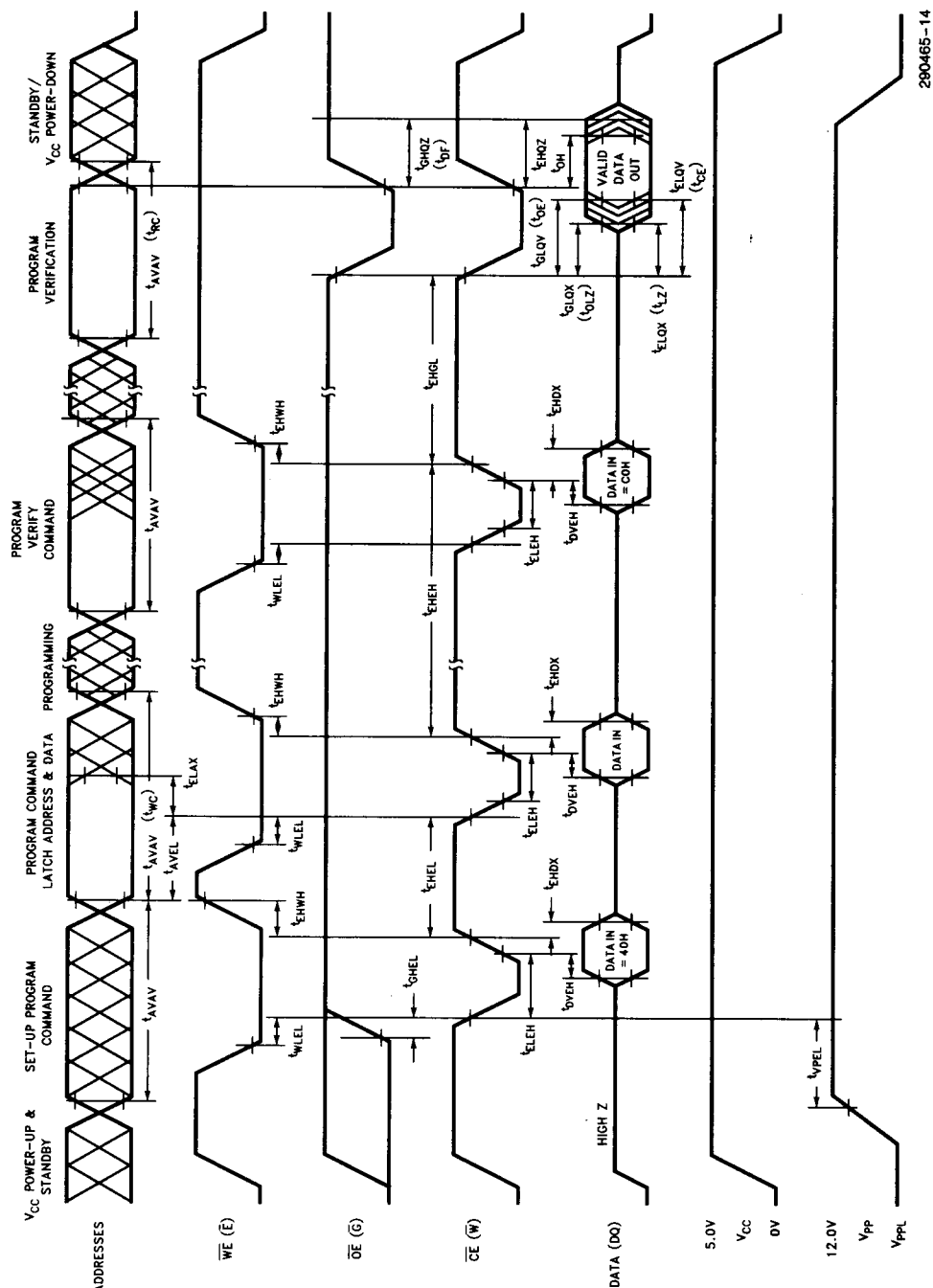
### Figure 13. AC Waveforms for Erase Operations

# ALTERNATIVE $\overline{\text{CE}}$ -CONTROLLED WRITES

Versions			28F020-150		Unit
Symbol	Characteristic	Notes	Min	Max	
$t_{\text{AVAV}}$	Write Cycle Time		150		ns
$t_{\text{AVEL}}$	Address Set-Up Time		0		ns
$t_{\text{ELAX}}$	Address Hold Time		80		ns
$t_{\text{DVEH}}$	Data Set-Up Time		50		ns
$t_{\text{EHDX}}$	Data Hold Time		10		ns
$t_{\text{EHGL}}$	Write Recovery Time before Read		6		$\mu\text{s}$
$t_{\text{GHEL}}$	Read Recovery Time before Write		0		$\mu\text{s}$
$t_{\text{WLEL}}$	Write Enable Set-Up Time before Chip Enable		0		ns
$t_{\text{EHWLH}}$	Write Enable Hold Time		0		ns
$t_{\text{ELEH}}$	Write Pulse Width	1	70		ns
$t_{\text{EHEL}}$	Write Pulse Width High		20		ns
$t_{\text{VPEL}}$	$V_{\text{PP}}$ Set-Up Time to Chip Enable Low		1.0		$\mu\text{s}$

## NOTE:

1. Chip-Enable Controlled Writes: Write operations are driven by the valid combination of Chip-Enable and Write-Enable. In systems where Chip-Enable defines the write pulse width (within a longer Write-Enable timing waveform) all set-up, hold and inactive Write-Enable times should be measured relative to the Chip-Enable waveform.



**NOTE:**  
Alternative  $\overline{\text{CE}}$ -Controlled Write Timings also apply to erase operations.

### Figure 14. Alternate AC Waveforms for Programming Operations

## **APPENDIX A**

### **PARTIAL LIST(1) OF 80-PIN SIMM SOCKET COMPANIES**

AMP INCORPORATED  
HARRISBURG, PA 17105  
(800) 522-6752

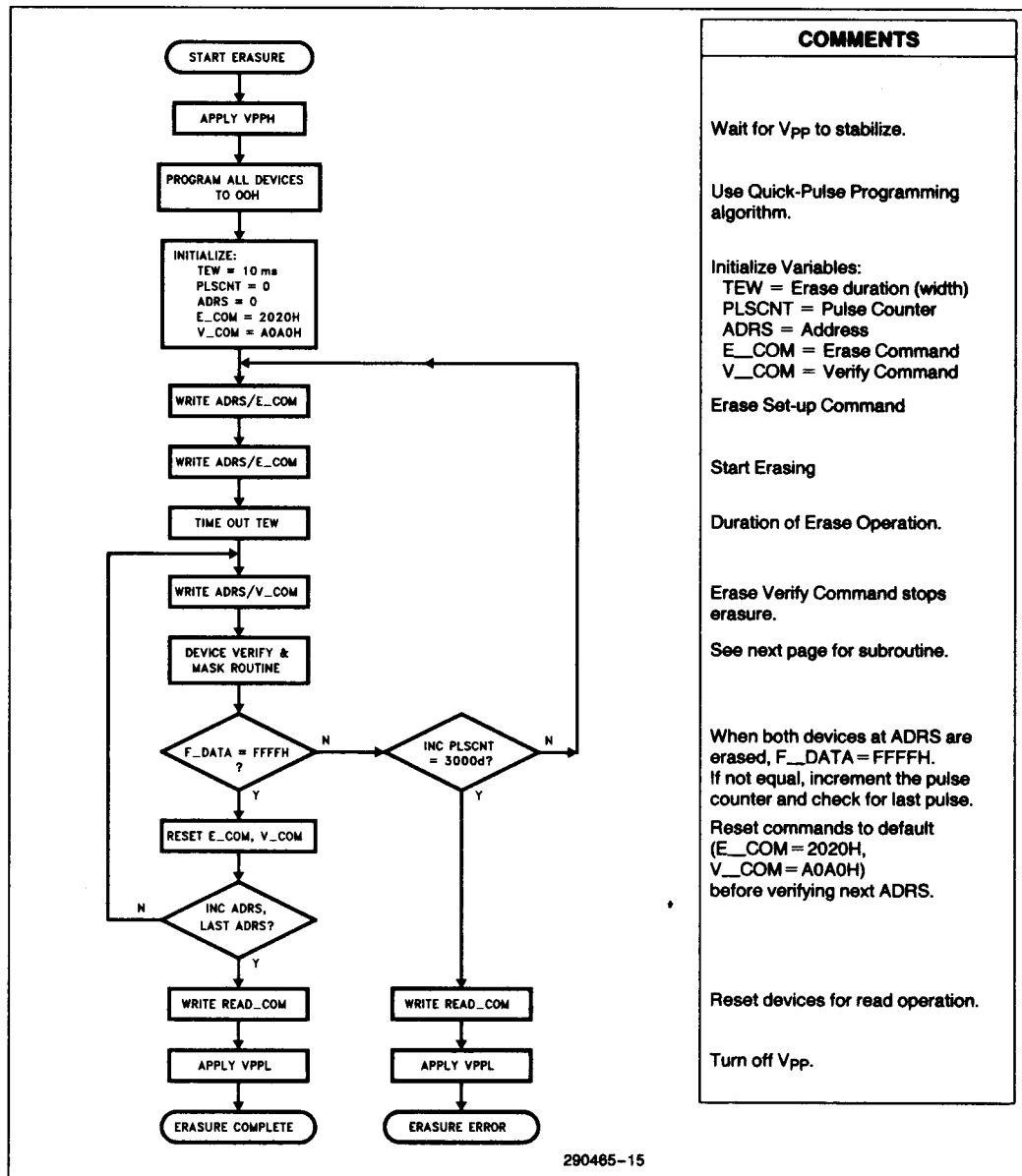
BURNDY CORPORATION  
51 RICHARDS AVENUE  
NORWALK, CT 06856  
(203) 838-4444

MOLEX  
2222 WELLINGTON COURT  
LISLE, IL 60532  
(708) 969-4550

**NOTES:**

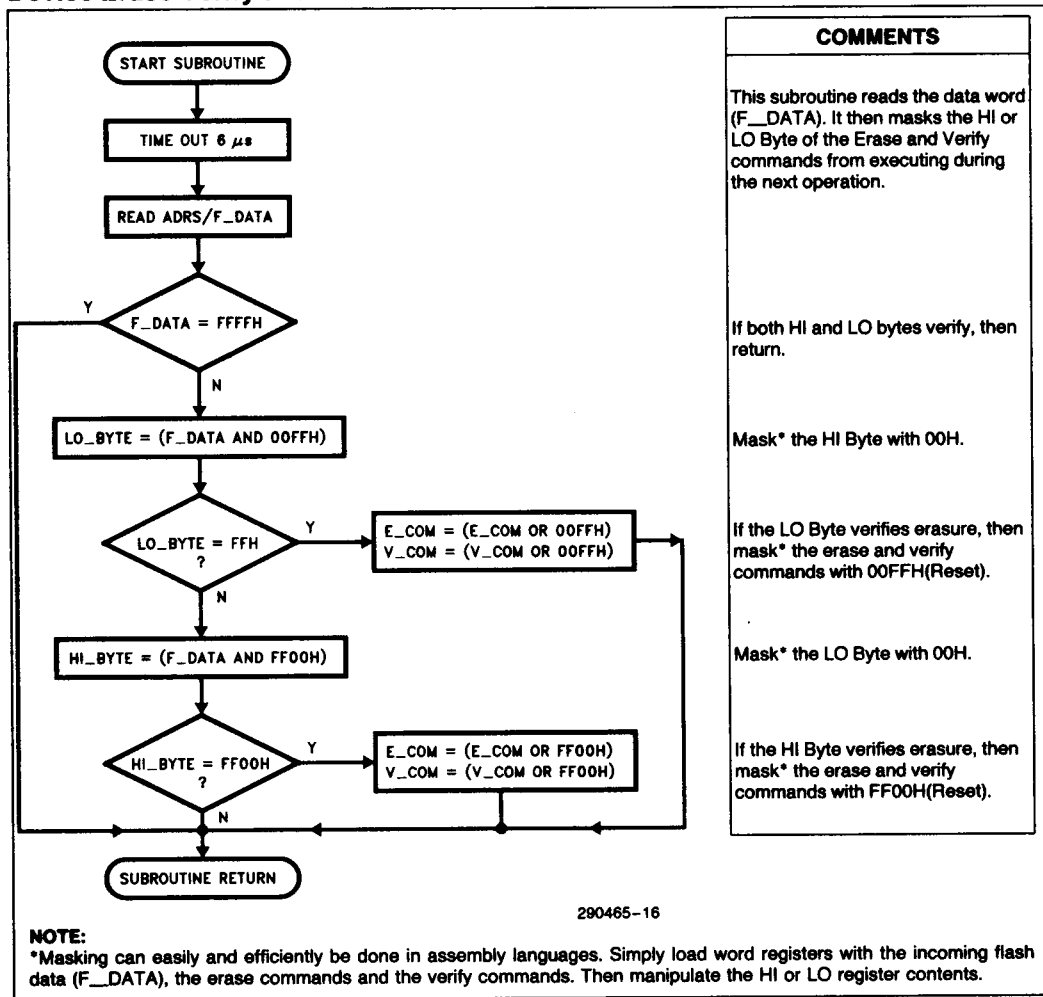
1. This list is intended for example only, and in no way represents all companies that support 80-pin SIMM Sockets. Intel Corporation assumes no responsibility for circuitry other than circuitry embodies in an Intel product. No other circuit patent licenses are implied.
2. Socket reliability data can be obtained from the above companies upon request.

## APPENDIX B PARALLEL ERASE FLOW CHART



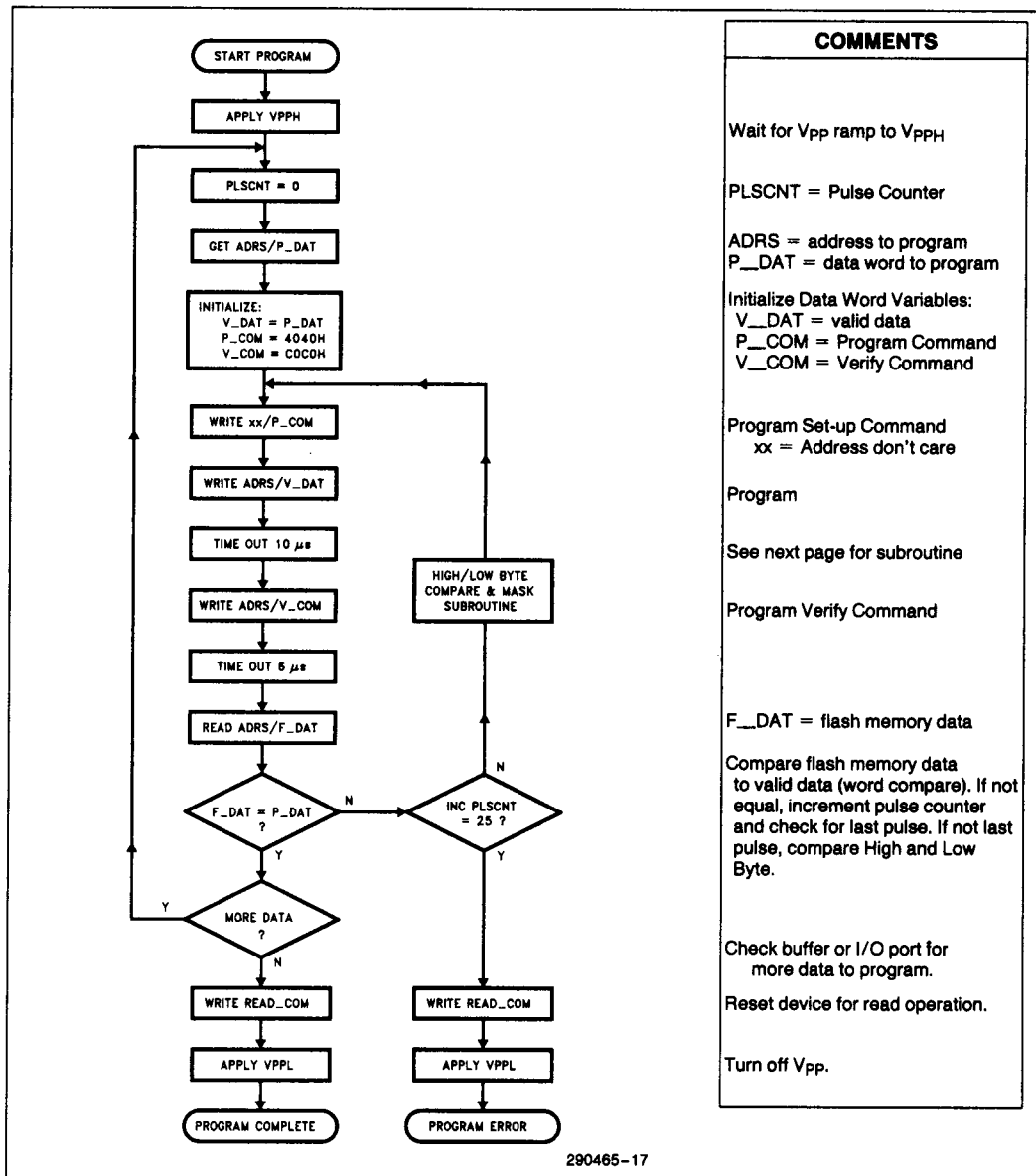


# Device Erase Verify and Mask Subroutine

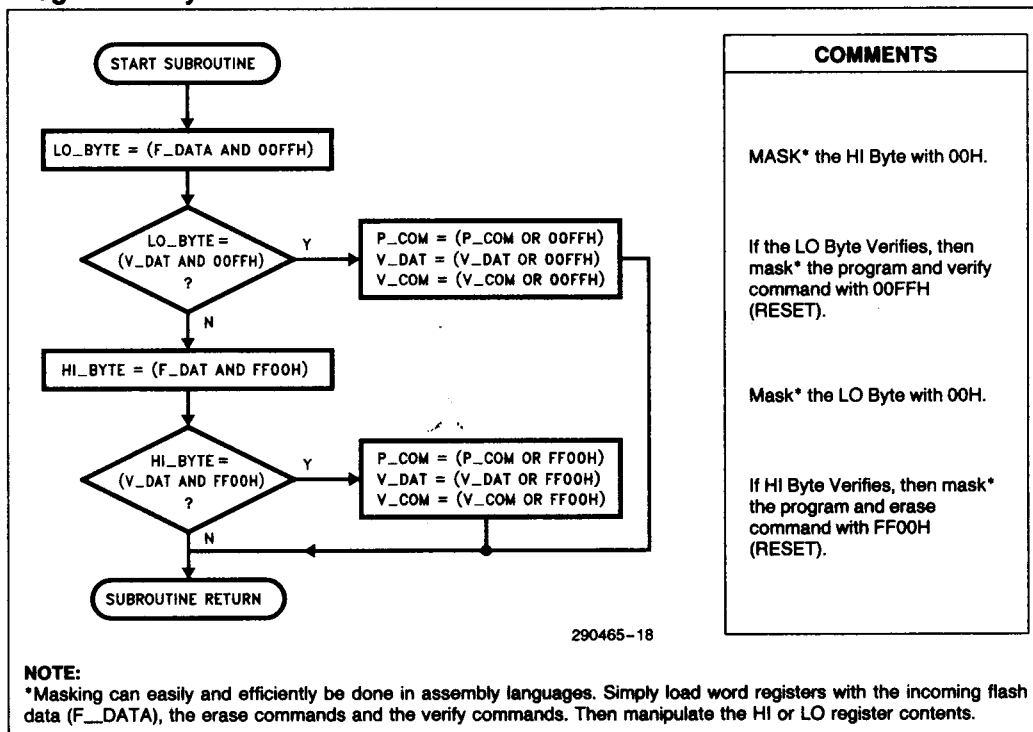


290465-16

## APPENDIX C PARALLEL PROGRAMMING FLOW CHART

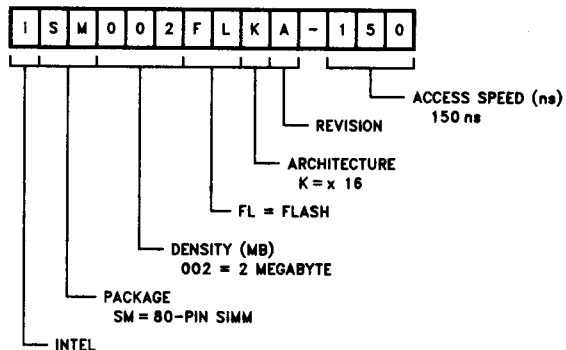


# Program Verify and Mask Subroutine



290465-18

## Ordering Information



290485-19

### Valid Combinations:

ISM002FLKA-150

## ADDITIONAL INFORMATION

### Order Number

ER-20, "ETOX™ II Flash Memory Technology"	294005
ER-24, "The Intel 28F020 Flash Memory"	294008
RR-60, "ETOX™ II Flash Memory Reliability Data Summary"	293002
AP-316, "Using Flash Memory for In-System Reprogrammable Nonvolatile Storage"	292046
AP-325, "Guide to Flash Memory Reprogramming"	292059
AP-343, "Flash Memory — A Mass Storage Medium"	292079